

## OSFP-800GB-2XFR4-LPO-AR-AO

Arista Networks® Compatible TAA 800GBase-2xFR4 PAM4 OSFP-IHS Transceiver (SMF, 1310nm, 2km, 2xLC, DOM, CMIS 5.0) LPO

### Features

- OSFP Package
- Duplex LC Receptacle Optical Connector
- 3.3V Power Supply
- 2x30 OSFP Electrical Interface
- Single-Mode Fiber
- Hot-Pluggable
- 1271nm/1291nm/1311nm/1331nm High-Power DFB Lasers, PIN PD Receiver
- Compliant to CMIS for 8-16x Pluggable Transceivers R5.2
- Operating Temperature: 0 to 70 Celsius
- 53GBaud Data Rate
- RoHS Compliant and Lead-Free



### Applications

- 2x400GBase Ethernet

### Product Description

This Arista Networks® compatible OSFP-IHS Transceiver provides 800GBase-2xFR4 throughput up to 2km over single-mode fiber (SMF) PAM4 using a wavelength of 1310nm via a 2xLC connector. It can operate at temperatures between 0 and 70C. All of our transceivers are built to comply with Multi-Source Agreement (MSA) standards and are uniquely serialized and tested for data-traffic and application to ensure seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."



### Absolute Maximum Ratings

| Parameter                     | Symbol | Min. | Max. | Unit | Notes |
|-------------------------------|--------|------|------|------|-------|
| Storage Ambient Temperature   | Tstg   | -40  | +85  | °C   |       |
| Relative Humidity – Storage   | RH     | 0    | 95   | %    | 1     |
| Relative Humidity – Operating | RH     | 0    | 85   | %    | 1     |
| Module Supply Voltage         | Vcc    | -0.5 | 3.6  | V    |       |

#### Notes:

1. RH is a non-condensing condition.
2. Exceeding the Absolute Maximum Ratings may cause irreversible damage to the device. The device is not intended to be operated under the condition of simultaneous Absolute Maximum Ratings, a condition which may cause irreversible damage to the device.

### Recommended Operating Conditions

| Parameter                    | Symbol | Min.  | Typ.   | Max.  | Unit    | Notes |
|------------------------------|--------|-------|--------|-------|---------|-------|
| Case Operating Temperature   | Tc     | 0     | +25    | 70    | °C      | 1     |
| Module Supply Voltage        | Vcc    | 3.135 | 3.3    | 3.465 | V       |       |
| Power Consumption            | PC     |       |        | 8.5   | W       |       |
| PAM4 Signaling Rate Per Lane | S      |       | 53.125 |       | GBaud/s | 2     |

#### Notes:

1. Temperature range = C.
2. Range: ±100ppm.

## Electrical Characteristics

| Parameter                             | Symbol | Min. | Typ.   | Max. | Unit     | Notes |
|---------------------------------------|--------|------|--------|------|----------|-------|
| Transmitter                           |        |      |        |      |          |       |
| Tx_Data VMA                           | VMA    | 175  |        | 350  | mV       | 1     |
|                                       | VMA    | 200  |        | 350  | mV       | 2     |
| Tx_Data EECQ                          | EECQ   |      |        | 3.5  | dB       | 1     |
|                                       | EECQ   |      |        | 3.0  | dB       | 2     |
| Tx_Data Ceeq                          | Ceeq   | -0.5 |        | 0.75 | dB       | 1     |
|                                       | Ceeq   | -0.5 |        | 0.5  | dB       | 2     |
| Receiver                              |        |      |        |      |          |       |
| Rx_Data Differential Output Voltage   | VOUT   |      |        | 800  | mV       |       |
| Rx_Data Differential Output Impedance | ZOUT   |      | 100    |      | $\Omega$ |       |
| Signaling Rate Per Lane               | S      |      | 53.125 |      | GBaud/s  | 3     |

### Notes:

1. Loss>13dB.
2. Loss≤13dB.
3. Range: ±100ppm.

## Optical Characteristics

| Parameter                                               | Symbol    | Min.                  | Typ. | Max.   | Unit | Notes |
|---------------------------------------------------------|-----------|-----------------------|------|--------|------|-------|
| Transmitter                                             |           |                       |      |        |      |       |
| PAM4 Signal Rate                                        | SR        | 53.125 ± 100ppm       |      |        | GBd  |       |
| Laser Type                                              |           | High-Power DFB Lasers |      |        |      |       |
| Lane Wavelength                                         | $\lambda$ | 1264.5                | 1271 | 1277.5 | nm   |       |
|                                                         |           | 1284.5                | 1291 | 1297.5 | nm   |       |
|                                                         |           | 1304.5                | 1311 | 1317.5 | nm   |       |
|                                                         |           | 1324.5                | 1331 | 1337.5 | nm   |       |
| Total Average Launch Power                              | Pt        |                       |      | 10.4   | dBm  |       |
| Average Launch Power Per Lane                           | POUT      | -3.2                  |      | 4.4    | dBm  | 1     |
| Outer Optical Modulation Amplitude                      | OMAuter   | -0.3                  |      | 3.7    | dBm  |       |
| Transmitter and Dispersion Penalty Eye Closure for PAM4 | TDECQ     |                       |      | 3.4    | dB   | 2     |
| Optical Output with Tx Off                              | Poff      |                       |      | -15    | dBm  | 3     |
| Extinction Ratio                                        | ER        | 2.5                   |      |        | dB   | 2     |
| Transmit Reflectance                                    | RFL       |                       |      | -26    | dB   |       |
| Receiver                                                |           |                       |      |        |      |       |
| PAM4 Signal Rate                                        | SR        | 53.125 ± 100ppm       |      |        | GBd  |       |
| Lane Wavelength                                         | $\lambda$ | 1264.5                | 1271 | 1277.5 | nm   |       |
|                                                         |           | 1284.5                | 1291 | 1297.5 | nm   |       |
|                                                         |           | 1304.5                | 1311 | 1317.5 | nm   |       |
|                                                         |           | 1324.5                | 1331 | 1337.5 | nm   |       |
| Average Receive Power                                   | PIN       | -7.2                  |      | 4.4    | dBm  | 3, 4  |
| Damage Threshold                                        |           | 5.4                   |      |        | dBm  | 3     |
| Receiver Sensitivity (OMAuter) Per Lane                 | Sen       | Max. (-4.6, SECQ-6.0) |      |        | dBm  | 5     |
| Receive Reflectance                                     | RFL       |                       |      | -26    | dB   |       |

### Notes:

1. Average optical output.
2. Test with SSPRQ pattern.
3. Each lane.
4. Average receive power, per lane (minimum), is informative and not the principal indicator of signal strength. A receive power below this value can't be compliant; however, a value above this does not ensure compliance.
5. BER =  $2.4e^{-4}$ , PAM4 signaling rate (each lane) 53.125GBaud, and PRBS  $2^{31}-1$ .

## Pin Descriptions

| Pin | Symbol    | Name/Description                   | Logic       | Direction       | Plug Sequence | Notes |
|-----|-----------|------------------------------------|-------------|-----------------|---------------|-------|
| 1   | GND       | Module Ground.                     |             |                 | 1             |       |
| 2   | Tx2p      | CH2 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3             |       |
| 3   | Tx2n      | CH2 Transmitter Data Inverted.     | CML-I       | Input from Host | 3             |       |
| 4   | GND       | Module Ground.                     |             |                 | 1             |       |
| 5   | Tx4p      | CH4 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3             |       |
| 6   | Tx4n      | CH4 Transmitter Data Inverted.     | CML-I       | Input from Host | 3             |       |
| 7   | GND       | Module Ground.                     |             |                 | 1             |       |
| 8   | Tx6p      | CH6 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3             |       |
| 9   | Tx6n      | CH6 Transmitter Data Inverted.     | CML-I       | Input from Host | 3             |       |
| 10  | GND       | Module Ground.                     |             |                 | 1             |       |
| 11  | Tx8p      | CH8 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3             |       |
| 12  | Tx8n      | CH8 Transmitter Data Inverted.     | CML-I       | Input from Host | 3             |       |
| 13  | GND       | Module Ground.                     |             |                 | 1             |       |
| 14  | SCL       | 2-Wire Serial Interface Clock.     | LVC MOS-I/O | Bi-Directional  | 3             | 1     |
| 15  | Vcc       | +3.3V Power Supply.                |             | Power from Host | 2             |       |
| 16  | Vcc       | +3.3V Power Supply.                |             | Power from Host | 2             |       |
| 17  | LPWn/PRSn | Low-Power Mode/Module Present.     | Multi-Level | Bi-Directional  | 3             | 2     |
| 18  | GND       | Module Ground.                     |             |                 | 1             |       |
| 19  | Rx7n      | CH7 Receiver Data Inverted.        | CML-O       | Output to Host  | 3             |       |
| 20  | Rx7p      | CH7 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3             |       |
| 21  | GND       | Module Ground.                     |             |                 | 1             |       |
| 22  | Rx5n      | CH5 Receiver Data Inverted.        | CML-O       | Output to Host  | 3             |       |
| 23  | Rx5p      | CH5 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3             |       |
| 24  | GND       | Module Ground.                     |             |                 | 1             |       |
| 25  | Rx3n      | CH3 Receiver Data Inverted.        | CML-O       | Output to Host  | 3             |       |
| 26  | Rx3p      | CH3 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3             |       |
| 27  | GND       | Module Ground.                     |             |                 | 1             |       |
| 28  | Rx1n      | CH1 Receiver Data Inverted.        | CML-O       | Output to Host  | 3             |       |
| 29  | Rx1p      | CH1 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3             |       |
| 30  | GND       | Module Ground.                     |             |                 | 1             |       |
| 31  | GND       | Module Ground.                     |             |                 | 1             |       |
| 32  | Rx2p      | CH2 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3             |       |
| 33  | Rx2n      | CH2 Receiver Data Inverted.        | CML-O       | Output to Host  | 3             |       |
| 34  | GND       | Module Ground.                     |             |                 | 1             |       |

|    |          |                                    |             |                 |   |   |
|----|----------|------------------------------------|-------------|-----------------|---|---|
| 35 | Rx4p     | CH4 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3 |   |
| 36 | Rx4n     | CH4 Receiver Data Inverted.        | CML-O       | Output to Host  | 3 |   |
| 37 | GND      | Module Ground.                     |             |                 | 1 |   |
| 38 | Rx6p     | CH6 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3 |   |
| 39 | Rx6n     | CH6 Receiver Data Inverted.        | CML-O       | Output to Host  | 3 |   |
| 40 | GND      | Module Ground.                     |             |                 | 1 |   |
| 41 | Rx8p     | CH8 Receiver Data Non-Inverted.    | CML-O       | Output to Host  | 3 |   |
| 42 | Rx8n     | CH8 Receiver Data Inverted.        | CML-O       | Output to Host  | 3 |   |
| 43 | GND      | Module Ground.                     |             |                 | 1 |   |
| 44 | INT/RSTn | Module Interrupt/Module Reset.     | Multi-Level | Bi-Directional  | 3 | 3 |
| 45 | Vcc      | +3.3V Power Supply.                |             | Power from Host | 2 |   |
| 46 | Vcc      | +3.3V Power Supply.                |             | Power from Host | 2 |   |
| 47 | SDA      | 2-Wire Serial Interface Data.      | LVC MOS-I/O | Bi-Directional  | 3 | 1 |
| 48 | GND      | Module Ground.                     |             |                 | 1 |   |
| 49 | Tx7n     | CH7 Transmitter Data Inverted.     | CML-I       | Input from Host | 3 |   |
| 50 | Tx7p     | CH7 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3 |   |
| 51 | GND      | Module Ground.                     |             |                 | 1 |   |
| 52 | Tx5n     | CH5 Transmitter Data Inverted.     | CML-I       | Input from Host | 3 |   |
| 53 | Tx5p     | CH5 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3 |   |
| 54 | GND      | Module Ground.                     |             |                 | 1 |   |
| 55 | Tx3n     | CH3 Transmitter Data Inverted.     | CML-I       | Input from Host | 3 |   |
| 56 | Tx3p     | CH3 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3 |   |
| 57 | GND      | Module Ground.                     |             |                 | 1 |   |
| 58 | Tx1n     | CH1 Transmitter Data Inverted.     | CML-I       | Input from Host | 3 |   |
| 59 | Tx1p     | CH1 Transmitter Data Non-Inverted. | CML-I       | Input from Host | 3 |   |
| 60 | GND      | Module Ground.                     |             |                 | 1 |   |

**Notes:**

1. Open-drain with pull-up resistor on the host.
2. LPWn/PRSn is a dual function signal that allows the host to signal low-power mode and allows the module to indicate that the module is present.
3. INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module.

Pin-Out Details

Top Side (viewed from top)

|    |          |  |
|----|----------|--|
| 60 | GND      |  |
| 59 | TX1p     |  |
| 58 | TX1n     |  |
| 57 | GND      |  |
| 56 | TX3p     |  |
| 55 | TX3n     |  |
| 54 | GND      |  |
| 53 | TX5p     |  |
| 52 | TX5n     |  |
| 51 | GND      |  |
| 50 | TX7p     |  |
| 49 | TX7n     |  |
| 48 | GND      |  |
| 47 | SDA      |  |
| 46 | VCC      |  |
| 45 | VCC      |  |
| 44 | INT/RSTn |  |
| 43 | GND      |  |
| 42 | RX8n     |  |
| 41 | RX8p     |  |
| 40 | GND      |  |
| 39 | RX6n     |  |
| 38 | RX6p     |  |
| 37 | GND      |  |
| 36 | RX4n     |  |
| 35 | RX4p     |  |
| 34 | GND      |  |
| 33 | RX2n     |  |
| 32 | RX2p     |  |
| 31 | GND      |  |

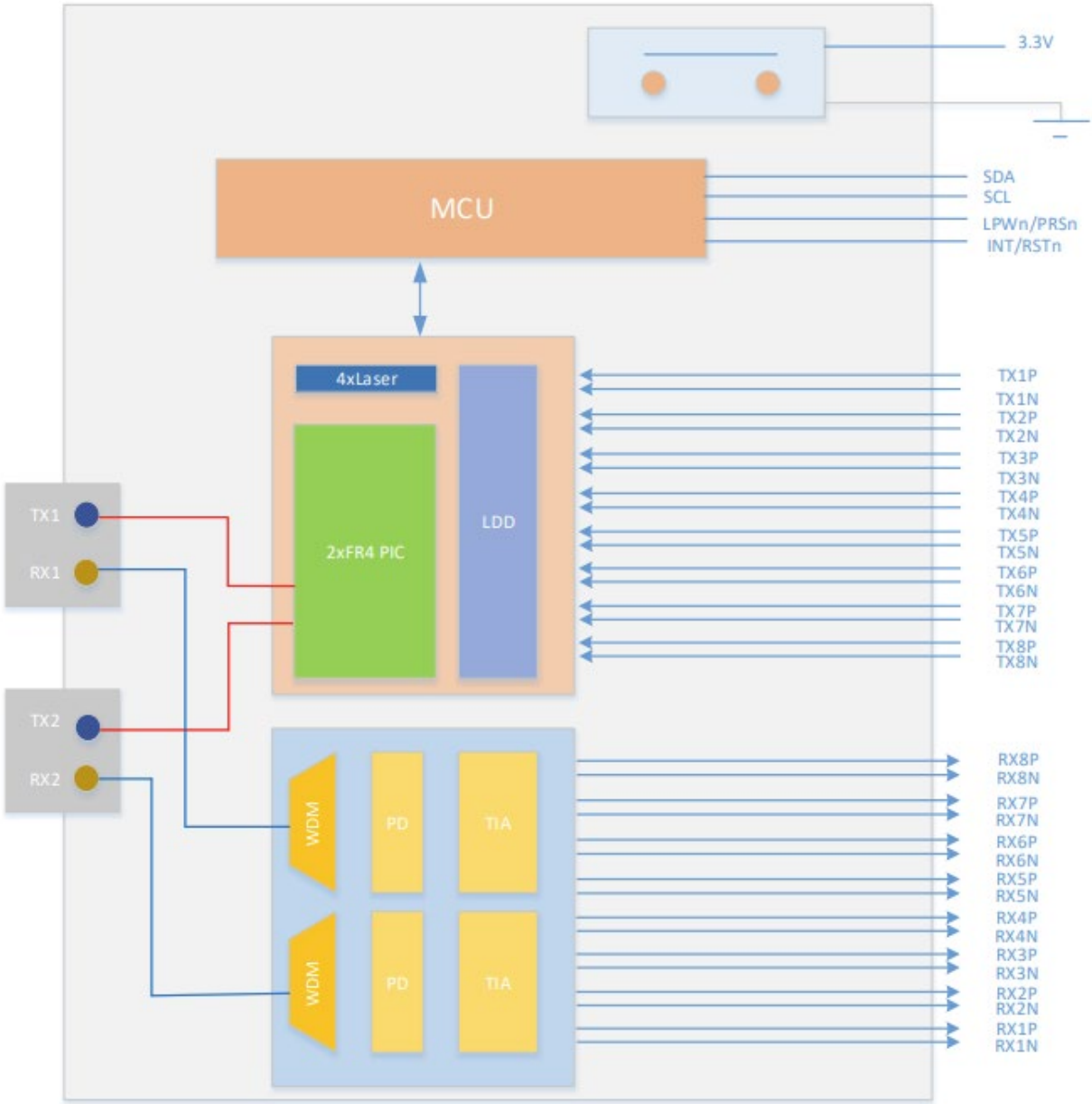
----- Module Card Edge -----

Bottom Side (viewed from bottom)

|  |           |    |
|--|-----------|----|
|  | GND       | 1  |
|  | TX2p      | 2  |
|  | TX2n      | 3  |
|  | GND       | 4  |
|  | TX4p      | 5  |
|  | TX4n      | 6  |
|  | GND       | 7  |
|  | TX6p      | 8  |
|  | TX6n      | 9  |
|  | GND       | 10 |
|  | TX8p      | 11 |
|  | TX8n      | 12 |
|  | GND       | 13 |
|  | SCL       | 14 |
|  | VCC       | 15 |
|  | VCC       | 16 |
|  | LPWn/PRSn | 17 |
|  | GND       | 18 |
|  | RX7n      | 19 |
|  | RX7p      | 20 |
|  | GND       | 21 |
|  | RX5n      | 22 |
|  | RX5p      | 23 |
|  | GND       | 24 |
|  | RX3n      | 25 |
|  | RX3p      | 26 |
|  | GND       | 27 |
|  | RX1n      | 28 |
|  | RX1p      | 29 |
|  | GND       | 30 |

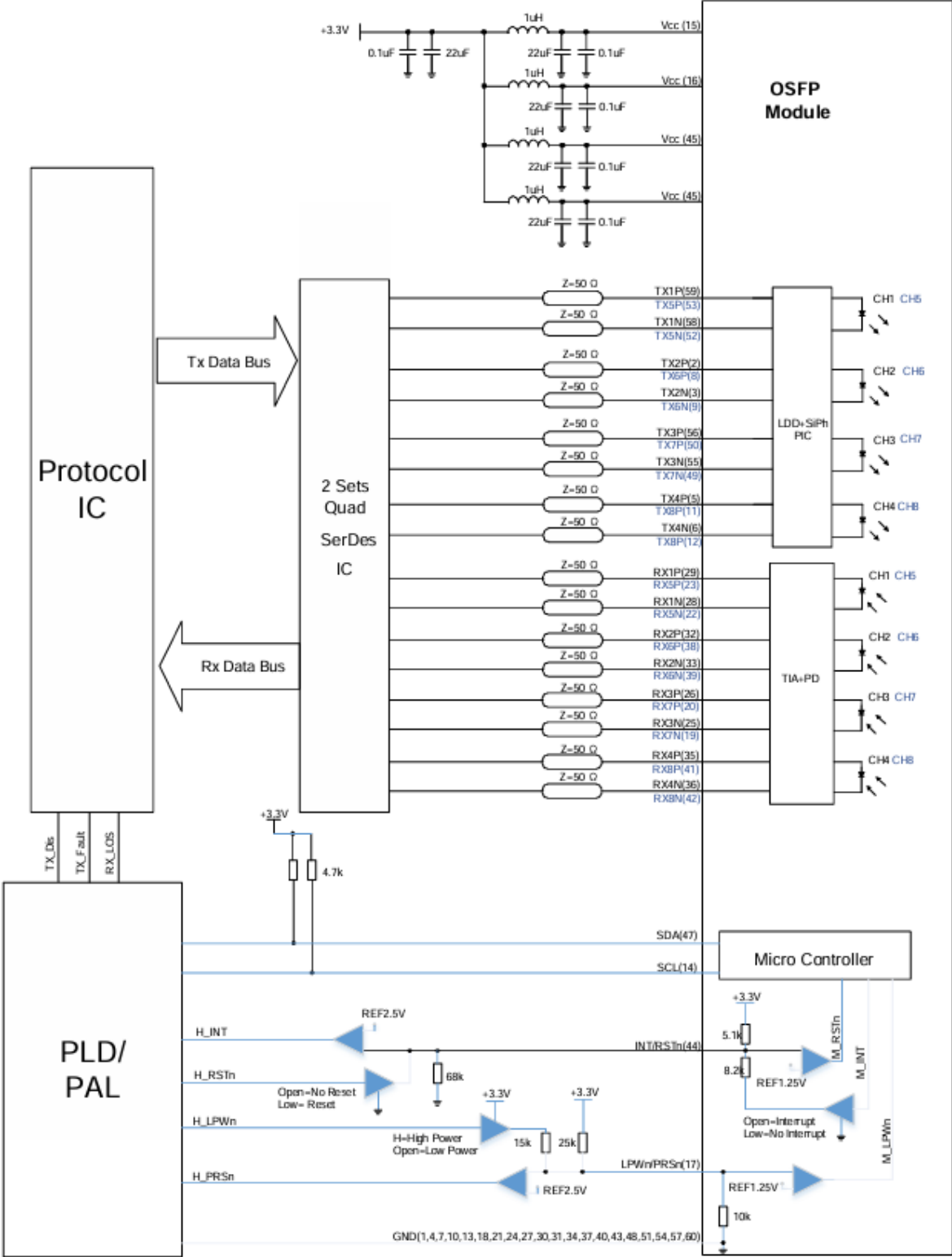
Block Diagram

Dual Duplex LC

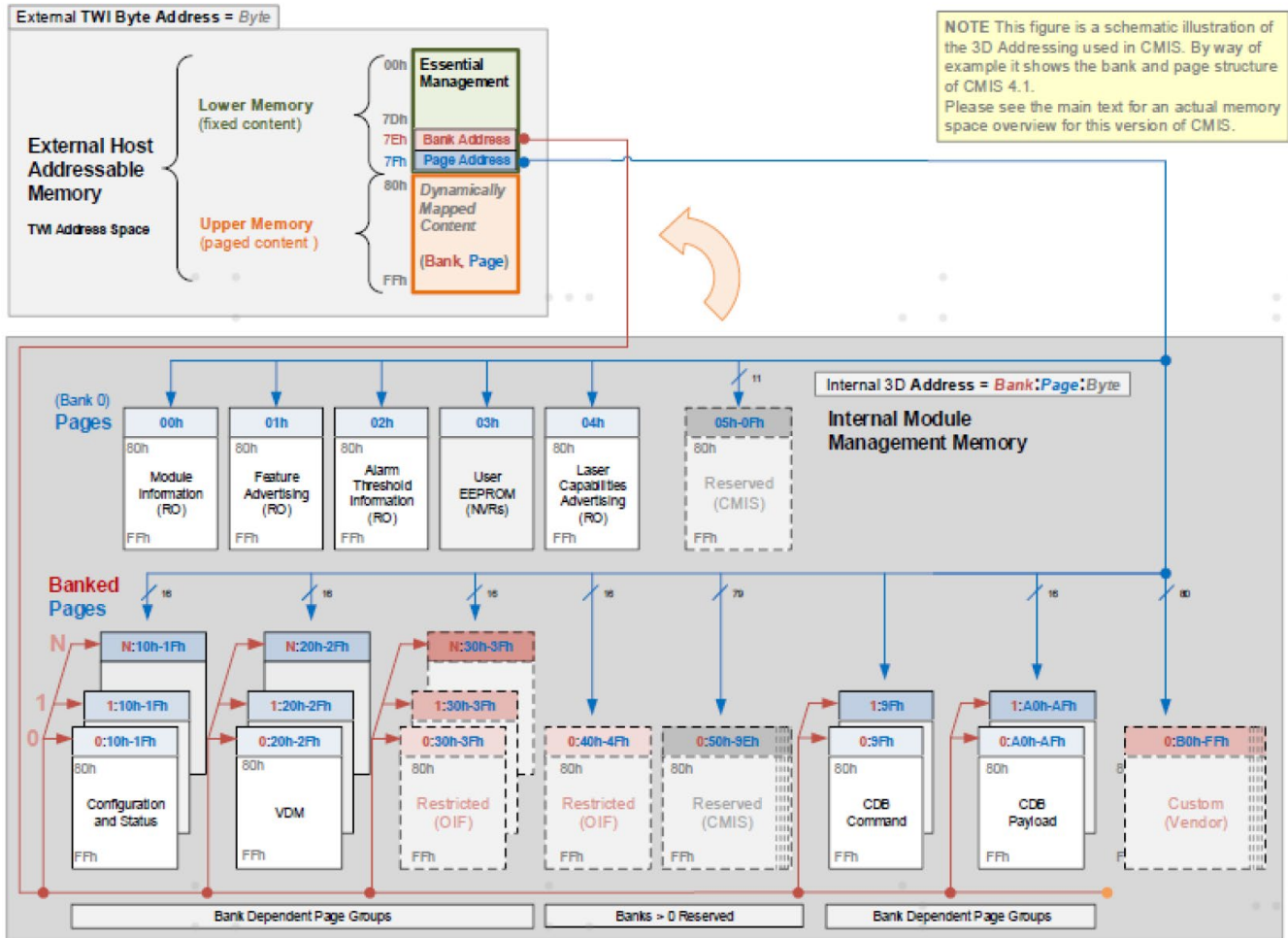




Host Board and Module Board Diagram



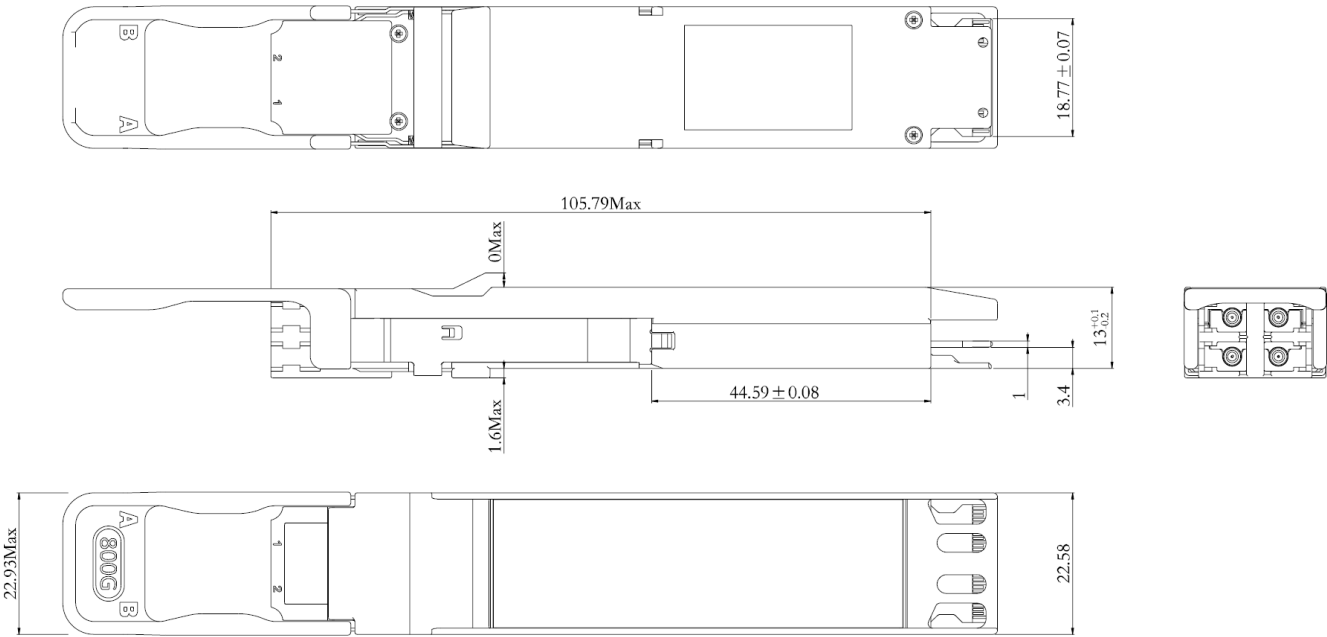
## 2-Wire Serial Memory Map



### Notes:

1. For detail definition of the registers, please refer to Common Management Interface Specifications for 8/16x Pluggable Transceivers, R5.2.

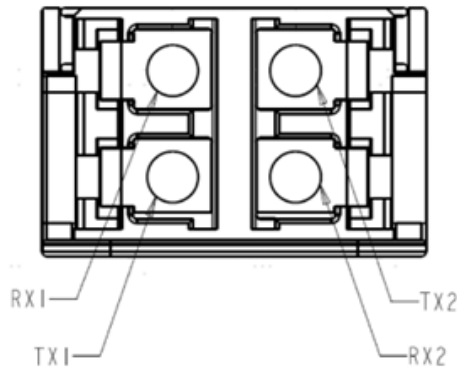
# Mechanical Specifications



## Notes:

- 1. Tolerance:  $\pm 0.1 \text{ mm}$ .
- 2. Others according with OSFP MSA or Customer Spec.
- 3. Light Port according with fiber connector spec.

# Optical Lane Assignment



## About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.



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