QSFP28-100GB-CWDM4-I-AR-AO

Arista Networks® Compatible TAA 100GBase-CWDM4 QSFP28 Transceiver (SMF, 1270nm to 1330nm, 2km, LC, DOM, -40 to 85C)

Features:

- Supports CPRI V7.0 Option 7/8/9/10
- Up to 2km over SMF
- Supports 40/100Gbps
- Power Dissipation:
- Duplex LC Receptacles
- 4x25G Electrical Interface
- PIN and TIA Array on the Receiver Side
- 4*25Gbps DFB-Based CWDM Transmitter
- Operating Temperature: -40 to 85 Celsius
- Single 3.3V Power Supply
- RoHS Complaint and Lead-Free

Applications:

- Ethernet over CWDM
- Access, Metro and Enterprise

Product Description

This Arista Networks® compatible QSFP28 transceiver provides 100GBase-CWDM4 throughput up to 2km over single-mode fiber (SMF) using wavelengths between 1270nm to 1330nm via an LC connector. It is capable of withstanding rugged environments and can operate at temperatures between -40 and 85C. Our transceiver is built to meet or exceed OEM specifications and is guaranteed to be 100% compatible with Arista Networks®. It has been programmed, uniquely serialized, and tested for data-traffic and application to ensure that it will initialize and perform identically. All of our transceivers comply with Multi-Source Agreement (MSA) standards to provide seamless network integration. Additional product features include Digital Optical Monitoring (DOM) support which allows access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."

TAA COMPLIANT

Absolute Maximum Ratings

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature		Tstg	-45		+100	°C	
Relative Humidity		RH	5		85	%	
Power Supply Voltage		Vcc	-0.5	3.3	3.6	V	
Data Input Voltage	**Single-Ended**		-0.5		Vcc+0.5	V	
	Differential				0.8	V	1
Receiver Damage Threshold Per Lane		RxDmg	3.5			dBm	

Notes:

1. This is the maximum voltage that can be applied across the differential inputs without damaging the input circuitry. The damage threshold of the module input shall be at least 1600mV peak to peak differential.
2. Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

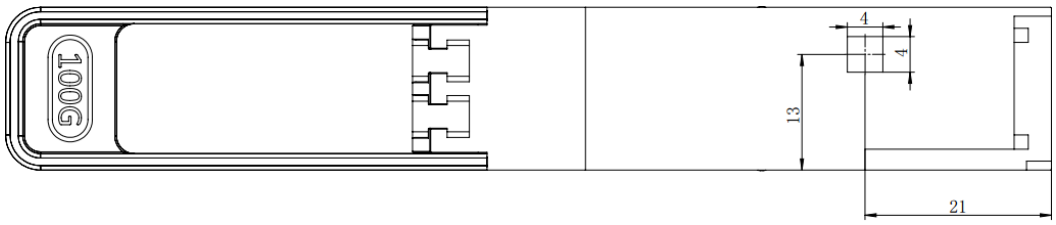
Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	Tc	-40	25	+85	°C	5
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Supply Noise				66	mVp-p	2
Power Dissipation	PD			4.5	W	
Electrical Signaling Rate Per Channel			25.78125		GBd	3
Optical Signaling Rate Per Channel			25.78125		GBd	4
Receiver Differential Data Output Load		100			Ω	

Notes:

1. Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP28 MSA Power Classification.
2. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply.
3. CAUI-4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.
4. 100G FR4 operation with Host generated FEC. The transmitter must receive pre-coded FEC signals from the host ASIC.

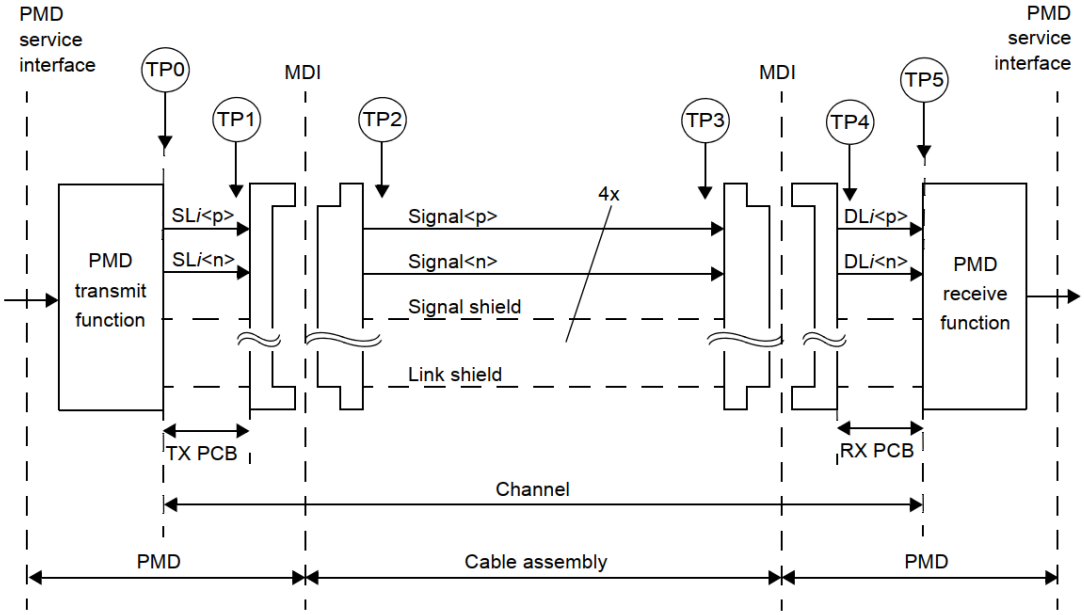
5. The position of case temperature measurement is shown below. Continuous operation at the maximum Recommended Operating Case Temperature should be avoided in order not to degrade reliability. The below picture shows the location of the hottest spot for measuring module case temperature. In addition, the digital diagnostic monitors (DDM) temperature is also calibrated to this spot. All dimensions in mm.



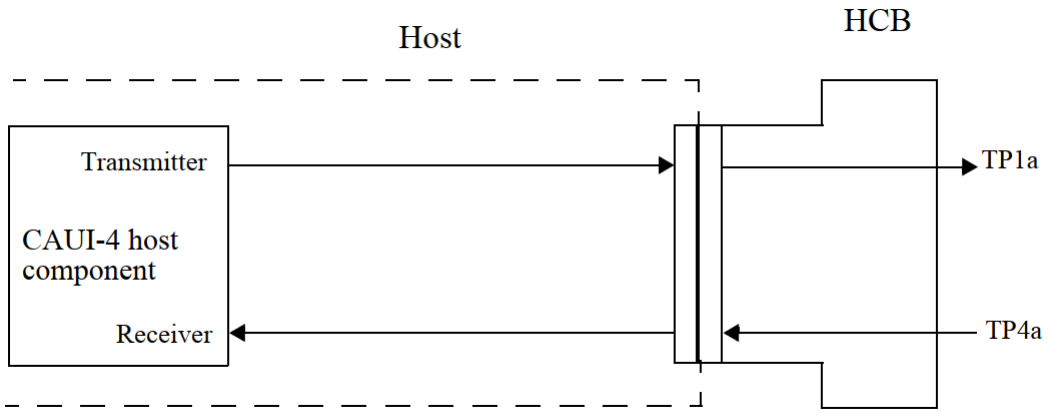
Reference Points

Test Point	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4.
TP0 to TP2 **TP3 to TP5**	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3bj 92.8.3 and 92.8.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3bj 92.8.3.6
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3bj table 92.6 are made at TP2 utilizing the test fixture specified in 802.3bj 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3bj 92.8.4 are made at TP3 utilizing the test fixture specified in 802.3bj 92.11.1.

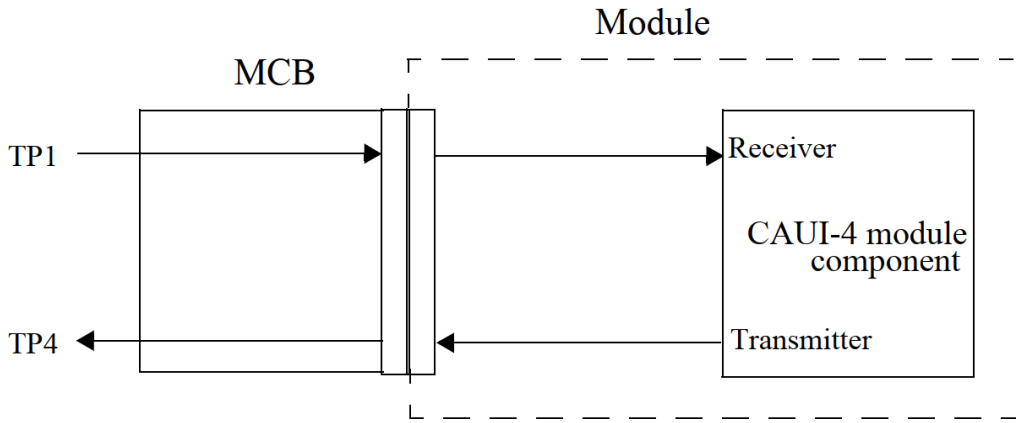
IEEE 802.3bj 100GBASE-CR4 Link



IEEE 802.3bm CAUI-4 Compliance Points TP1a, TP4a



IEEE 802.3bm CAUI-4 Compliance Points TP1, TP4



Electrical Characteristics

Parameter	Symbol/ Test Point	Min.	Typ.	Max.	Unit	Notes
Transceiver Power Consumption				4.5	W	
Transceiver Power Supply Total Current				1440	mA	
AC Coupling Capacitors (Internal)			0.1		µF	
High Speed Electrical Input						
Signaling Rate Per Lane	TP1		25.78125		GBd	±100ppm
Differential Pk-Pk Input Voltage Tolerance	TP1a	900			mV	
Single-Ended Voltage Tolerance Range	TP1a	-0.4		3.3	V	
DC Common-Mode Output Voltage	TP1	-350		2850	mV	1
Differential Input Return Loss (Minimum)	TP1	Equation (83E-5)			dB	802.3bm
Differential- to Common-Mode Input Return Loss (Minimum)	TP1	Equation (83E-6)			dB	802.3bm
Differential Termination Mismatch	TP1			10	%	

Module Stressed Input Test	TP1a					2
Eye Width			0.46		UI	
Applied Pk-Pk Sinusoidal Jitter			Table 88-13			
Eye Height			95		mV	
High Speed Electrical Output						
Signaling Rate Per Lane	TP4	25.78125 ± 100ppm			GBd	
AC Common-Mode Output Voltage (RMS)	TP4		17.5		mV	
DC Common-Mode Voltage	TP4	-350		2850	mV	1
Differential Output Voltage	TP4			900	mV	
Differential Output Return Loss (Minimum)	TP4	Equation (83E-2)			dB	
Common- to Differential-Mode Conversion Return Loss (Minimum)	TP4	Equation (83E-3)			dB	
Differential Termination Mismatch	TP4			10	%	
Transition Time (20-80%)	TP4	12			ps	
Eye Width	TP4	0.57			UI	
Eye Height Differential	TP4	228			mV	
Vertical Eye Closure	TP4			5.5	dB	

Notes:

1. DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.
2. Module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1.

Control Interface Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL and SDA	VOL	0		0.4	V
SCL and SDA	VIL	-0.3		Vcc*0.3	V
	VIH	Vcc*0.7		Vcc+0.5	V
LPMode/TxDis, ResetL, ModSelL	VIL	-0.3		0.8	V
	VIH	2		Vcc+0.3	V
LPMode, ResetL, ModSelL	|Iin|			360	µA
IntL/RxLOSL	VOL	0		0.4	V
	VOH	Vcc-0.5		Vcc+0.3	V
ModPrsL	VOL	0		0.4	V

Optical Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter @TP2 Test Point							
Signaling Speed Per Lane		BRave		25.78125		Gbps	
Data Rate Variation			-100		+100	ppm	
Modulation Format				NRZ			
Center Wavelength	**Lane_0**	λC0	1264.5		1277.5	nm	
	Lane_1	λC1	1284.5		1297.5	nm	
	Lane_2	λC2	1304.5		1317.5	nm	
	Lane_3	λC3	1324.5		1337.5	nm	
Total Average Output Power		PO			8.5	dBm	
Average Launch Power Per Lane		Peach	-6.5		2.5	dBm	1
Transmit OMA Per Lane		TxOMA	-4.0		2.5	dBm	2
Launch Power in OMA Minus TDP Per Lane		OMA-TDP	-5.0			dBm	
Transmitter and Dispersion Penalty Per Lane		TDP			3	dB	3
Side-Mode Suppression Ratio		SMSR	30			dB	
-20dB Spectrum Width		SW-20			1	nm	
Optical Return Loss Tolerance					20	dB	
Transmitter Reflectance					-12	dB	4
Extinction Ratio		ER	3.5			dB	
Average Launch Power of Off Transmitter Per Lane		P_off			-30	dBm	
RIN OMA		RIN			-128	dB/Hz	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}			{0.31, 0.4, 0.45, 0.34, 0.38, 0.4}				5
Receiver @TP3 Test Point							
Signaling Speed Per Lane		Brave		25.78125		Gbps	
Data Rate Variation			-100		+100	ppm	
Damage Threshold		Rxdmg	3.5				
Center Wavelength	**Lane_0**	λC0	1264.5		1277.5	nm	
	Lane_1	λC1	1284.5		1297.5	nm	
	Lane_2	λC2	1304.5		1317.5	nm	
	Lane_3	λC3	1324.5		1337.5	nm	
Average Receive Power Per Lane			-11.5		2.5		6
Receive Power (OMA) Per Lane					2.5		
Unstressed Receiver Sensitivity (OMA) Per Lane					-10		7
Stressed Receiver Sensitivity (OMA) Per Lane					-7.3		8

Receiver Reflectance				-26		
Conditions Of Stressed Receiver Sensitivity Test						
Vertical Eye Closure		1.9				9
Stressed J2 Jitter		0.33				9
Stressed J4 Jitter		0.48				9
SRS Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.39, 0.5, 0.5, 0.39, 0.39, 0.4}				9
LOS Assert		-25				
LOS De-Assert				-12		
LOS Hysteresis		0.5				

Notes:

1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDP < 1.0dB, the OMA (minimum) must exceed this value.
3. TDP does not include a penalty for multi-path interference (MPI).
4. Transmitter reflectance is defined looking into the transmitter.
5. Hit ratio of $5x10^{-5}$.
6. Average receive power, per lane (minimum), is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
7. Sensitivity is specified at $5x10^{-5}$ BER.
8. Measured with conformance test signal at TP3 for BER = $5x10^{-5}$.
9. Vertical eye closure penalty, stressed eye J2 Jitter, stressed eye J4 Jitter, and SRS eye mask definition are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Pin Descriptions

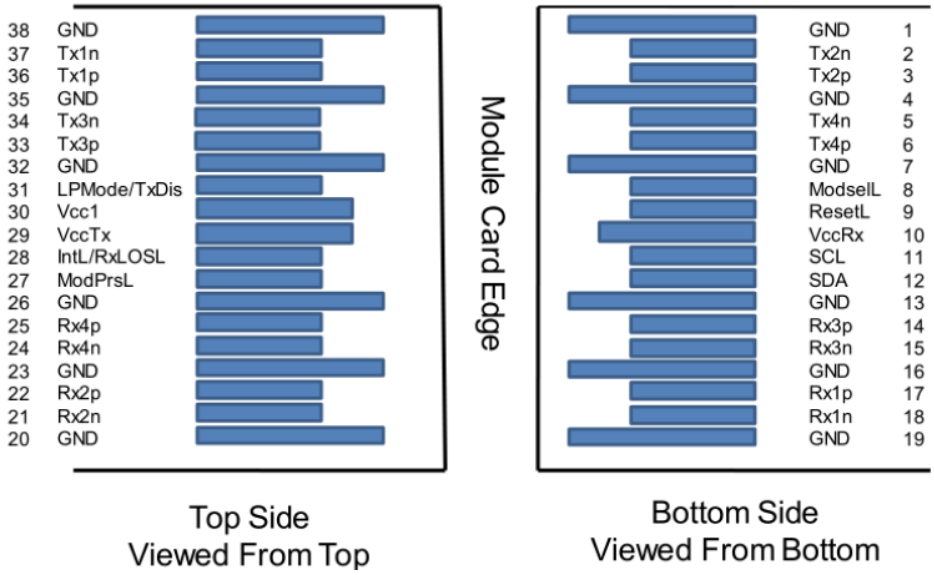
Pin	Logic	Symbol	Name/Description	Plug Sequence	Notes
1		GND	Module Ground.	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input.	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input.	3	
4		GND	Module Ground.	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input.	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input.	3	
7		GND	Module Ground.	1	1
8	LVTTL-I	ModSelL	Module Select.	3	
9	LVTTL-I	ResetL	Module Reset.	3	
10		VccRx	+3.3V Receiver Power Supply.	2	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3	
13		GND	Module Ground.	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output.	3	
15	CML-O	Rx3n	Receiver Inverted Data Output.	3	
16		GND	Module Ground.	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output.	3	
18	CML-O	Rx1n	Receiver Inverted Data Output.	3	
19		GND	Module Ground.	1	1
20		GND	Module Ground.	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output.	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output.	3	
23		GND	Module Ground.	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output.	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output.	3	
26		GND	Module Ground.	1	1
27	LVTTL-O	ModPrsL	Module Present.	3	
28	LVTTL-O	IntL/RxLOSL	Interrupt.	3	
29		VccTx	+3.3V Transmitter Power Supply.	2	2
30		Vcc1	+3.3V Power Supply.	2	2
31	LVTTL-I	LPMode/TxDis	Low-Power Mode.	3	
32		GND	Module Ground.	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input.	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input.	3	
35		GND	Module Ground.	1	1

36	CML-I	Tx1p	Transmitter Non-Inverted Data Input.	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input.	3	
38		GND	Module Ground.	1	1

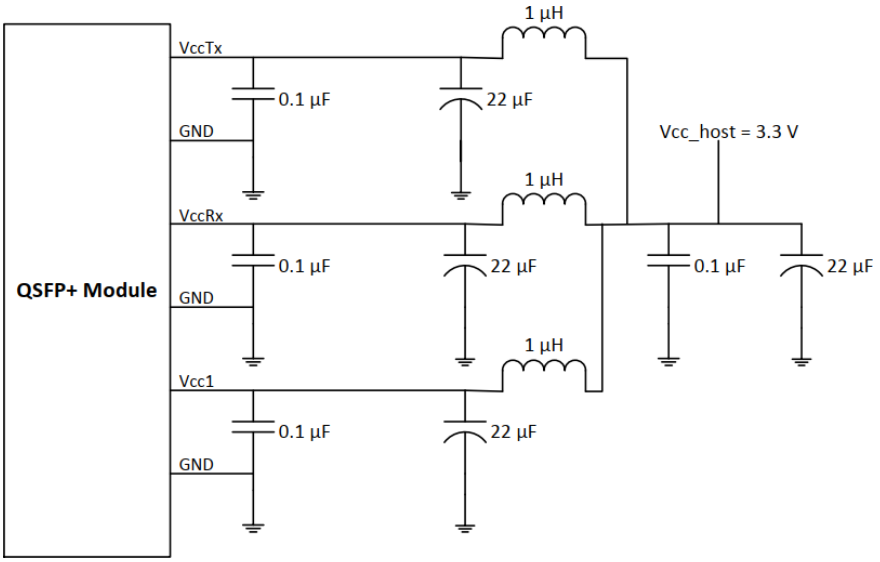
Notes:

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1, and VccTx are applied concurrently and may be internally connected within the module in any combination. Vcc contacts in SFF-8662 and SFF-8672 each have a steady state current rating of 1A.

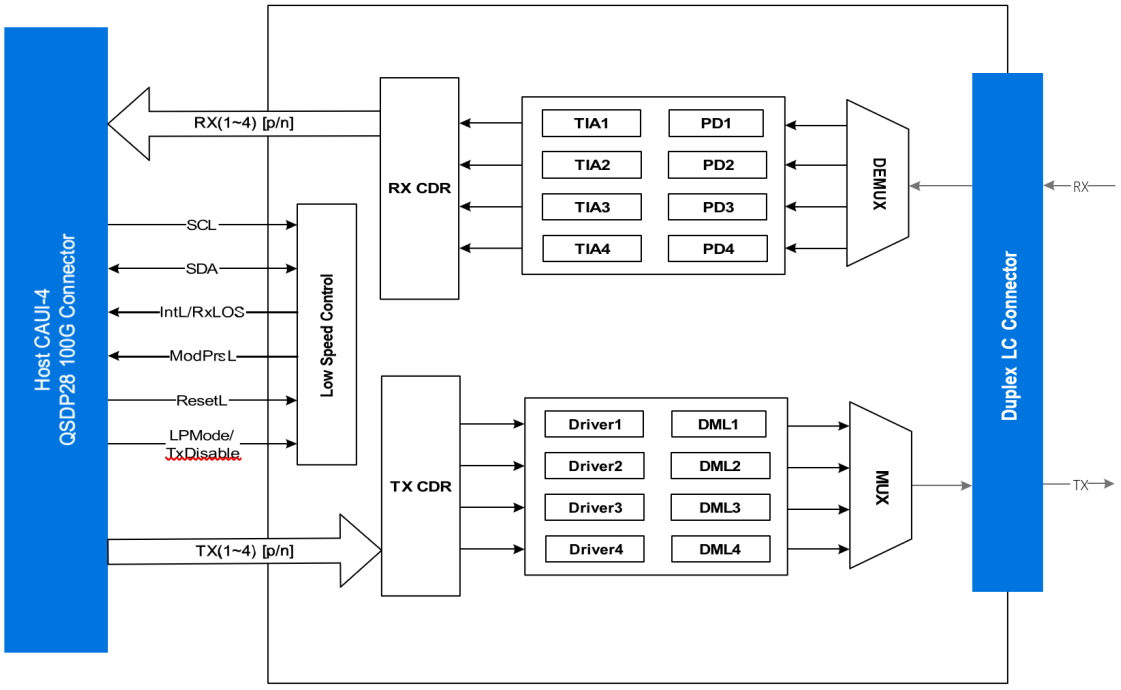
Electrical Pin-Out Details



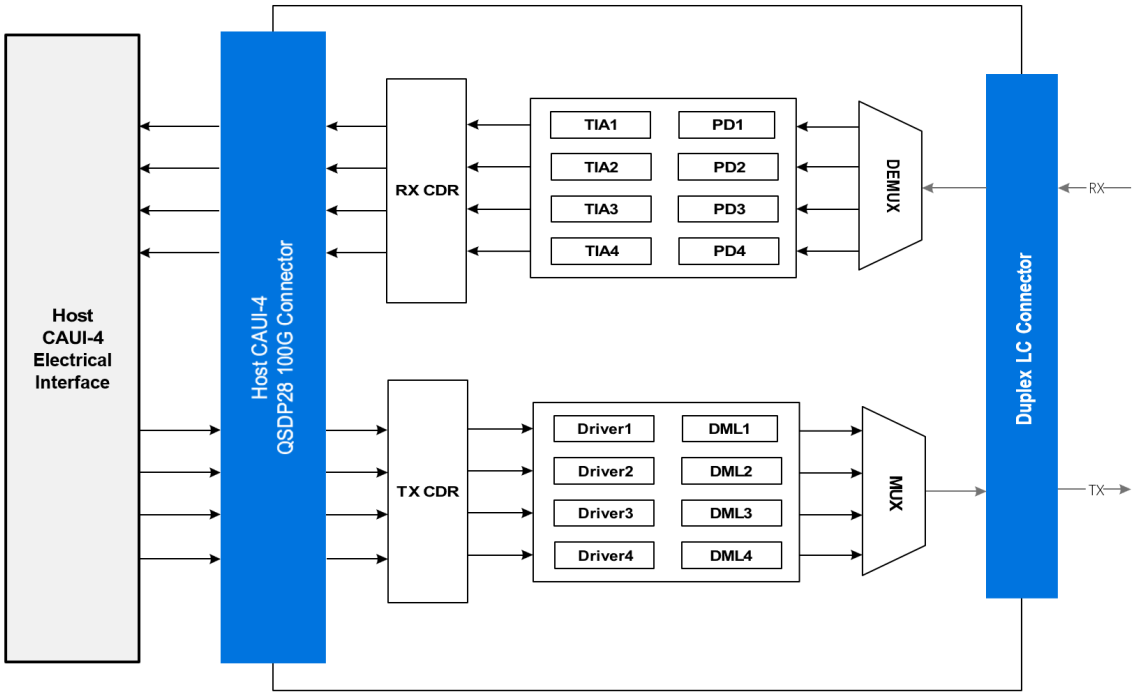
Host Board Power Supply Filter



Transceiver Block Diagram

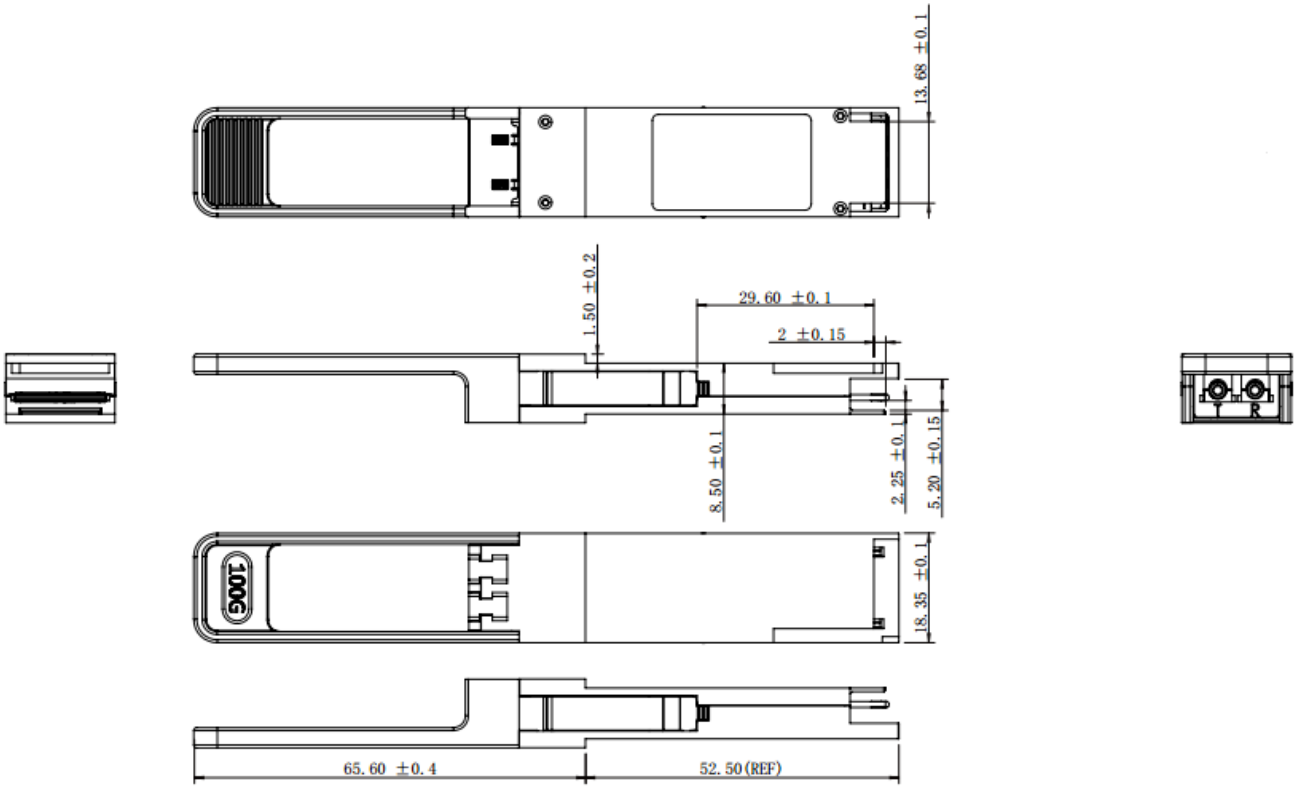


Application Reference Diagram

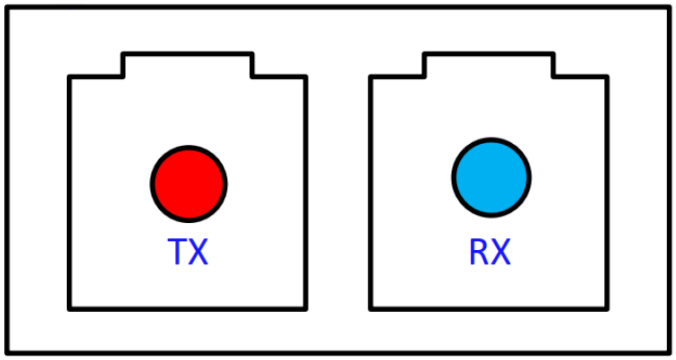


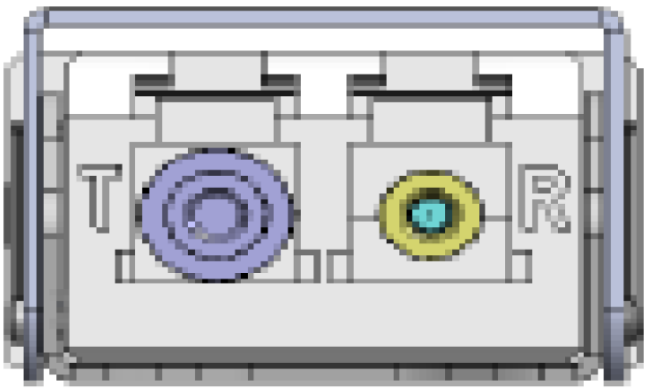
Mechanical Specifications

All dimension in mm.



Module Optical Interface (Looking into the Optical Port)





About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is ingrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications ranging from NEBS Level 3 to ISO 9001:2015 with every new development while maintaining the signature reliability of its products.

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