



### **Q400G-4Q56G-AOC5M-AR-OPC**

Arista Networks® Compatible 400GBase-AOC QSFP-DD to 4xQSFP56 PAM-4 Active Optical Cable (850nm, MMF, 5m) CMIS 3.0

#### **Features**

- Low latency DSP-free electronics-based CDR
- Multi-data rate up to 56.15 Gb/s per lane
- PAM4 modulation
- Single 3.3 V power supply
- Low power consumption: 7.6W on 400G end, 2.3W on 100G end with all CDRs enabled
- QSFP-DD MSA compliant
- CMIS 4.0 compliant
- Commercial temperature 0 to 70 Celsius
- Hot pluggable
- RoHS compliant and lead-free
- LSZH-rated cable
- IEEE 802.3cm



#### **Applications:**

- 400GBase Ethernet
- Data center: Switches, servers, storages and NIC adapters

#### **Product Description**

This is an Arista Networks® compatible TAA compliant 400GBase-CU QSFP-DD 400G to 4xQSFP56 100G active optical cable that operates over multi-mode fiber with a maximum reach of 5.0m (16.4ft). At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

OptioConnect's transceivers are RoHS compliant and lead-free.

### Absolute Maximum Ratings

| Parameter                  | Symbol  | Min. | Typ. | Max. | Unit | Notes   |
|----------------------------|---------|------|------|------|------|---------|
| Supply Voltage             | VIN     | 0    |      | 4.0  | V    |         |
| Input Swing                | VIN-MAX |      |      | 1500 | mVpp |         |
| Storage Temperature        | TSTG    | −40  |      | 85   | °C   | Ambient |
| Operating Case Temperature | Top     | 0    |      | 70   | °C   |         |
| Relative Humidity          | RH      | 5    |      | 85   | %    |         |

### Electrical Specifications

| Parameter                        |          | Symbol   | Min. | Typ.    | Max.                 | Unit | Notes |
|----------------------------------|----------|----------|------|---------|----------------------|------|-------|
| Data Rate (Per Channel)          |          | BR       |      | 26.5625 |                      | GBd  |       |
| Power Supply Voltage             |          | VCC      | 3.15 | 3.30    | 3.47                 | V    |       |
| Power Supply Current             | 400G End | ICC      |      | 2300    | 2500                 | mA   | 1     |
|                                  | 100G End | ICC      |      | 680     | 750                  | mA   | 1     |
| Power Consumption                | 400G End | P        |      | 7.6     | 8.0                  | W    | 1     |
|                                  | 100G End | P        |      | 2.3     | 2.5                  | W    | 1     |
| Transmitter                      |          |          |      |         |                      |      |       |
| Input Differential Impedance     |          | RIN      |      | 100     |                      | Ω    |       |
| Diff. Pk-Pk Input Vol. Tolerance |          | VINP-P   | 900  |         |                      | mV   |       |
| Receiver                         |          |          |      |         |                      |      |       |
| Output Differential Impedance    |          | ROUT     |      | 100     |                      | Ω    |       |
| Differential Data Output Swing   |          | VOU TP-P | 700  | 800     | 900                  | mV   |       |
| Bit Error Ratio (at 26.5625 GBd) |          |          |      |         | 2.4×10 <sup>-4</sup> |      | 3     |

### Notes:

1. Per end, all channel CDRs are enabled.
2. Pre-FEC Bit Error Ratio with a PRBS 231 – 1 test pattern over a normal operating temperature range.

### Pin Descriptions (QSFP-DD 400G End)

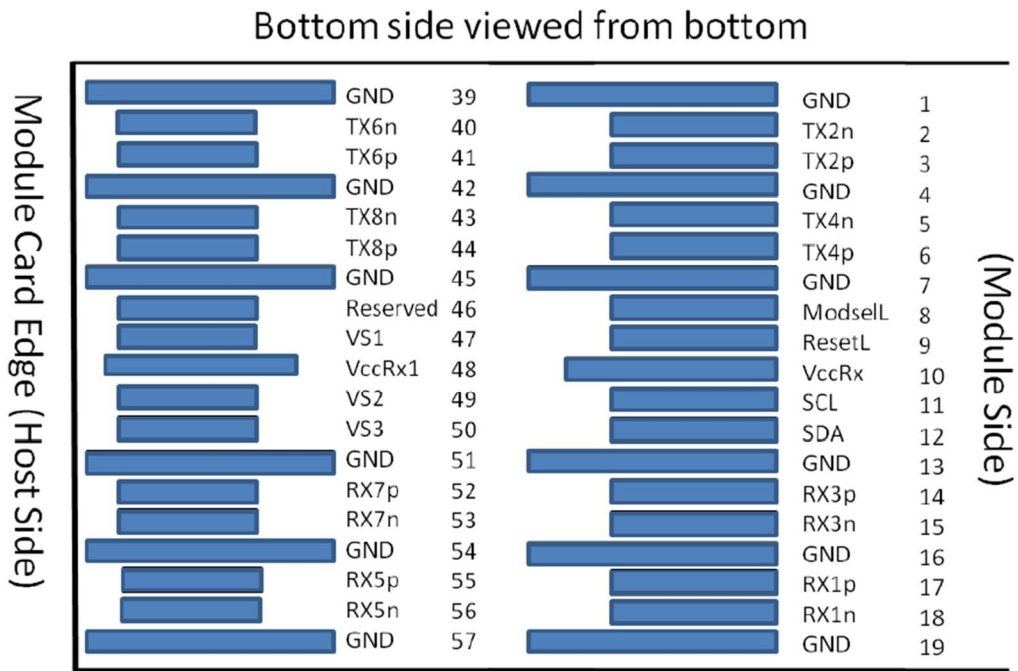
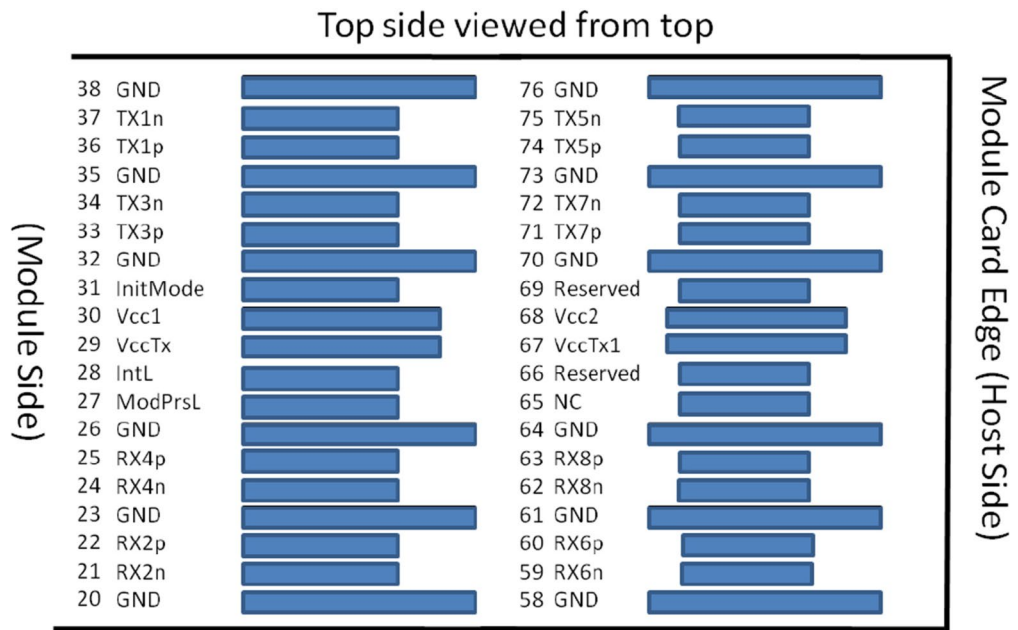
| PIN | Logic       | Symbol   | Description                                                                         | Notes |
|-----|-------------|----------|-------------------------------------------------------------------------------------|-------|
| 1   |             | GND      | Ground                                                                              | 1     |
| 2   | CML-I       | Tx2n     | Transmitter Inverted Data Input                                                     |       |
| 3   | CML-I       | Tx2p     | Transmitter Non-Inverted Data Input                                                 |       |
| 4   |             | GND      | Ground                                                                              | 1     |
| 5   | CML-I       | Tx4n     | Transmitter Inverted Data Input                                                     |       |
| 6   | CML-I       | Tx4p     | Transmitter Non-Inverted Data Input                                                 |       |
| 7   |             | GND      | Ground                                                                              | 1     |
| 8   | LVTTL-I     | ModSelL  | Module Select                                                                       |       |
| 9   | LVTTL-I     | ResetL   | Module Reset                                                                        |       |
| 10  |             | VccRx    | +3.3V Power Supply Receiver                                                         | 2     |
| 11  | LVC MOS-I/O | SCL      | 2-wire serial interface clock                                                       |       |
| 12  | LVC MOS-I/O | SDA      | 2-wire serial interface data                                                        |       |
| 13  |             | GND      | Ground                                                                              | 1     |
| 14  | CML-O       | Rx3p     | Receiver Non-Inverted Data Output                                                   |       |
| 15  | CML-O       | Rx3n     | Receiver Inverted Data Output                                                       |       |
| 16  |             | GND      | Ground                                                                              | 1     |
| 17  | CML-O       | Rx1p     | Receiver Non-Inverted Data Output                                                   |       |
| 18  | CML-O       | Rx1n     | Receiver Inverted Data Output                                                       |       |
| 19  |             | GND      | Ground                                                                              | 1     |
| 20  |             | GND      | Ground                                                                              | 1     |
| 21  | CML-O       | Rx2n     | Receiver Inverted Data Output                                                       |       |
| 22  | CML-O       | Rx2p     | Receiver Non-Inverted Data Output                                                   |       |
| 23  |             | GND      | Ground                                                                              | 1     |
| 24  | CML-O       | Rx4n     | Receiver Inverted Data Output                                                       |       |
| 25  | CML-O       | Rx4p     | Receiver Non-Inverted Data Output                                                   |       |
| 26  |             | GND      | Ground                                                                              | 1     |
| 27  | LVTTL-O     | ModPrsL  | Module Present                                                                      |       |
| 28  | LVTTL-O     | IntL     | Interrupt                                                                           |       |
| 29  |             | VccTx    | +3.3V Power Supply Transmitter                                                      | 2     |
| 30  |             | Vccl     | +3.3V Power Supply                                                                  | 2     |
| 31  | LVTTL-I     | InitMode | Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE |       |
| 32  |             | GND      | Ground                                                                              | 1     |
| 33  | CML-I       | Tx3p     | Transmitter Non-Inverted Data Input                                                 |       |
| 34  | CML-I       | Tx3n     | Transmitter Inverted Data Input                                                     |       |
| 35  |             | GND      | Ground                                                                              | 1     |
| 36  | CML-I       | Tx1p     | Transmitter Non-Inverted Data Input                                                 |       |
| 37  | CML-I       | Tx1n     | Transmitter Inverted Data Input                                                     |       |
| 38  |             | GND      | Ground                                                                              | 1     |

| PIN |       | Symbol   | Description                         | Notes |
|-----|-------|----------|-------------------------------------|-------|
| 39  |       | GND      | Ground                              | 1     |
| 40  | CML-I | Tx6n     | Transmitter Inverted Data Input     |       |
| 41  | CML-I | Tx6p     | Transmitter Non-Inverted Data Input |       |
| 42  |       | GND      | Ground                              | 1     |
| 43  | CML-I | Tx8n     | Transmitter Inverted Data Input     |       |
| 44  | CML-I | Tx8p     | Transmitter Non-Inverted Data Input |       |
| 45  |       | GND      | Ground                              | 1     |
| 46  |       | Reserved | For future use                      | 3     |
| 47  |       | VSI      | Module Vendor Specific 1            | 3     |
| 48  |       | VccRx1   | 3.3V Power Supply                   | 2     |
| 49  |       | VS2      | Module Vendor Specific 2            | 3     |
| 50  |       | VS3      | Module Vendor Specific 3            | 3     |
| 51  |       | GND      | Ground                              | 1     |
| 52  | CML-O | Rx7p     | Receiver Non-Inverted Data Output   |       |
| 53  | CML-O | Rx7n     | Receiver Inverted Data Output       |       |
| 54  |       | GND      | Ground                              | 1     |
| 55  | CML-O | Rx5p     | Receiver Non-Inverted Data Output   |       |
| 56  | CML-O | Rx5n     | Receiver Inverted Data Output       |       |
| 57  |       | GND      | Ground                              | 1     |
| 58  |       | GND      | Ground                              | 1     |
| 59  | CML-O | Rx6n     | Receiver Inverted Data Output       |       |
| 60  | CML-O | Rx6p     | Receiver Non-Inverted Data Output   |       |
| 61  |       | GND      | Ground                              | 1     |
| 62  | CML-O | Rx8n     | Receiver Inverted Data Output       |       |
| 63  | CML-O | Rx8p     | Receiver Non-Inverted Data Output   |       |
| 64  |       | GND      | Ground                              | 1     |
| 65  |       | NC       | No Connect                          | 3     |
| 66  |       | Reserved | For future use                      | 3     |
| 67  |       | VccTx1   | 3.3V Power Supply                   | 2     |
| 68  |       | Vcc2     | 3.3V Power Supply                   | 2     |
| 69  |       | Reserved | For future use                      | 3     |
| 70  |       | GND      | Ground                              | 1     |
| 71  | CML-I | Tx7p     | Transmitter Non-Inverted Data Input |       |
| 72  | CML-I | Tx7n     | Transmitter Inverted Data Input     |       |
| 73  |       | GND      | Ground                              | 1     |
| 74  | CML-I | Tx5p     | Transmitter Non-Inverted Data Input |       |
| 75  | CML-I | Tx5n     | Transmitter Inverted Data Input     |       |
| 76  |       | GND      | Ground                              | 1     |

**Notes:**

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Electrical Pin-out Details (QSFP-DD 400G End)



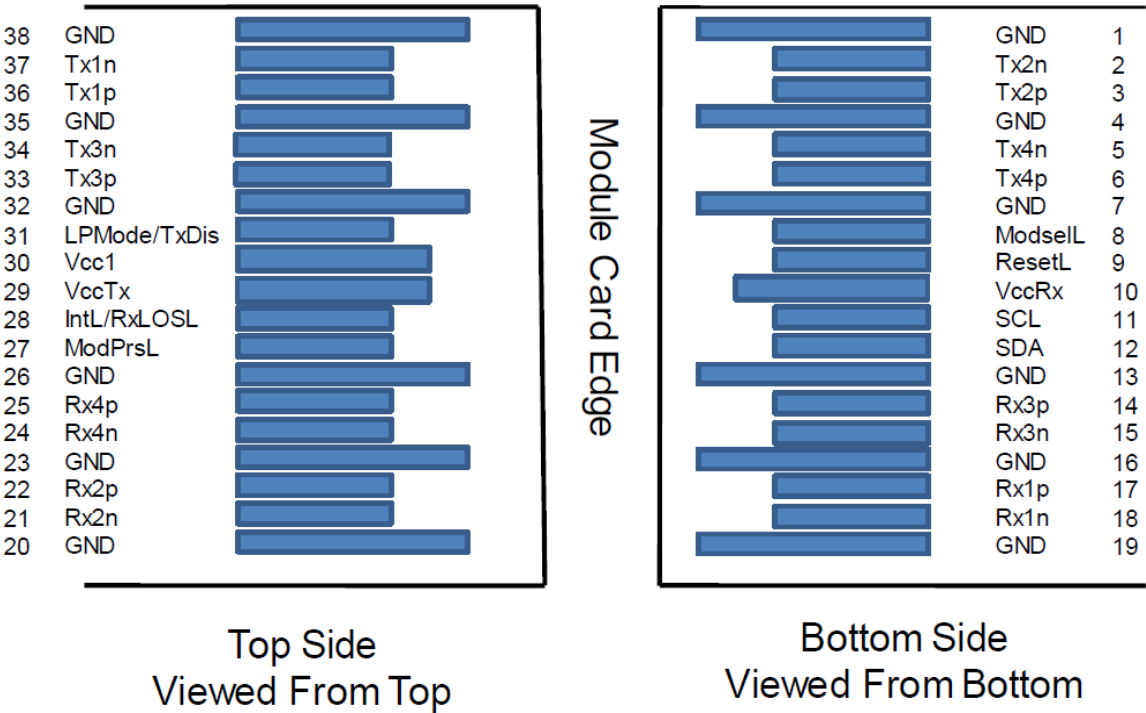
## Pin Descriptions (QSFP56 100G End)

| PIN | Logic       | Symbol  | Description                         | Notes |
|-----|-------------|---------|-------------------------------------|-------|
| 1   |             | GND     | Ground                              | 1     |
| 2   | CML-I       | Tx2n    | Transmitter Inverted Data Input     |       |
| 3   | CML-I       | Tx2p    | Transmitter Non-Inverted Data Input |       |
| 4   |             | GND     | Ground                              | 1     |
| 5   | CML-I       | Tx4n    | Transmitter Inverted Data Input     | 3     |
| 6   | CML-I       | Tx4p    | Transmitter Non-Inverted Data Input | 3     |
| 7   |             | GND     | Ground                              | 1     |
| 8   | LVTTL-I     | ModSelL | Module Select                       |       |
| 9   | LVTTL-I     | ResetL  | Module Reset                        |       |
| 10  |             | Vcc Rx  | +3.3V Power supply receiver         | 2     |
| 11  | LVC MOS-I/O | SCL     | 2-wire serial interface clock       |       |
| 12  | LVC MOS-I/O | SDA     | 2-wire serial interface data        |       |
| 13  |             | GND     | Ground                              | 1     |
| 14  | CML-O       | Rx3p    | Receiver Non-Inverted Data Output   | 3     |
| 15  | CML-O       | Rx3n    | Receiver Inverted Data Output       | 3     |
| 16  |             | GND     | Ground                              | 1     |
| 17  | CML-O       | Rx1p    | Receiver Non-Inverted Data Output   |       |
| 18  | CML-O       | Rx1n    | Receiver Inverted Data Output       |       |
| 19  |             | GND     | Ground                              | 1     |
| 20  |             | GND     | Ground                              | 1     |
| 21  | CML-O       | Rx2n    | Receiver Inverted Data Output       |       |
| 22  | CML-O       | Rx2p    | Receiver Non-Inverted Data Output   |       |
| 23  |             | GND     | Ground                              | 1     |
| 24  | CML-O       | Rx4n    | Receiver Inverted Data Output       | 3     |
| 25  | CML-O       | Rx4p    | Receiver Non-Inverted Data Output   | 3     |
| 26  |             | GND     | Ground                              | 1     |
| 27  | LVTTL-O     | ModPrsL | Module Present                      |       |
| 28  | LVTTL-O     | IntL    | Interrupt                           |       |
| 29  |             | Vcc Tx  | +3.3V Power supply transmitter      | 2     |
| 30  |             | Vcc 1   | +3.3V Power Supply                  | 2     |
| 31  | LVTTL-I     | LPMode  | Low Power Mode                      |       |
| 32  |             | GND     | Ground                              | 1     |
| 33  | CML-I       | Tx3p    | Transmitter Non-Inverted Data Input | 3     |
| 34  | CML-I       | Tx3n    | Transmitter Inverted Data Input     | 3     |
| 35  |             | GND     | Ground                              | 1     |
| 36  | CML-I       | Tx1p    | Transmitter Non-Inverted Data Input |       |
| 37  | CML-I       | Tx1n    | Transmitter Inverted Data Input     |       |
| 38  |             | GND     | Ground                              | 1     |

**Notes:**

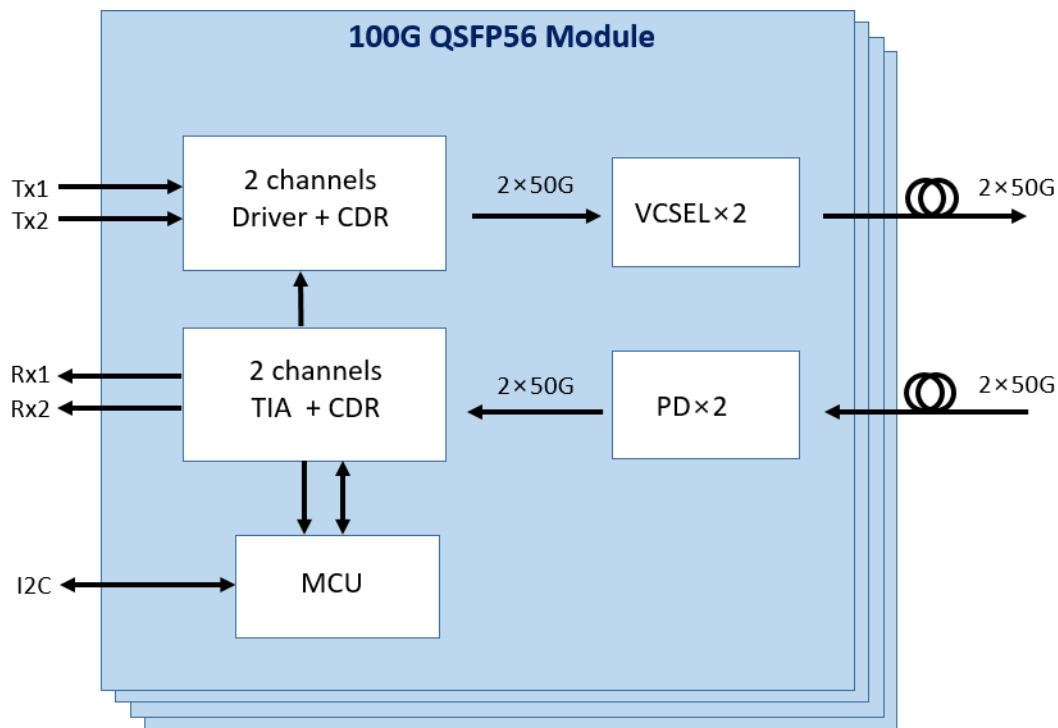
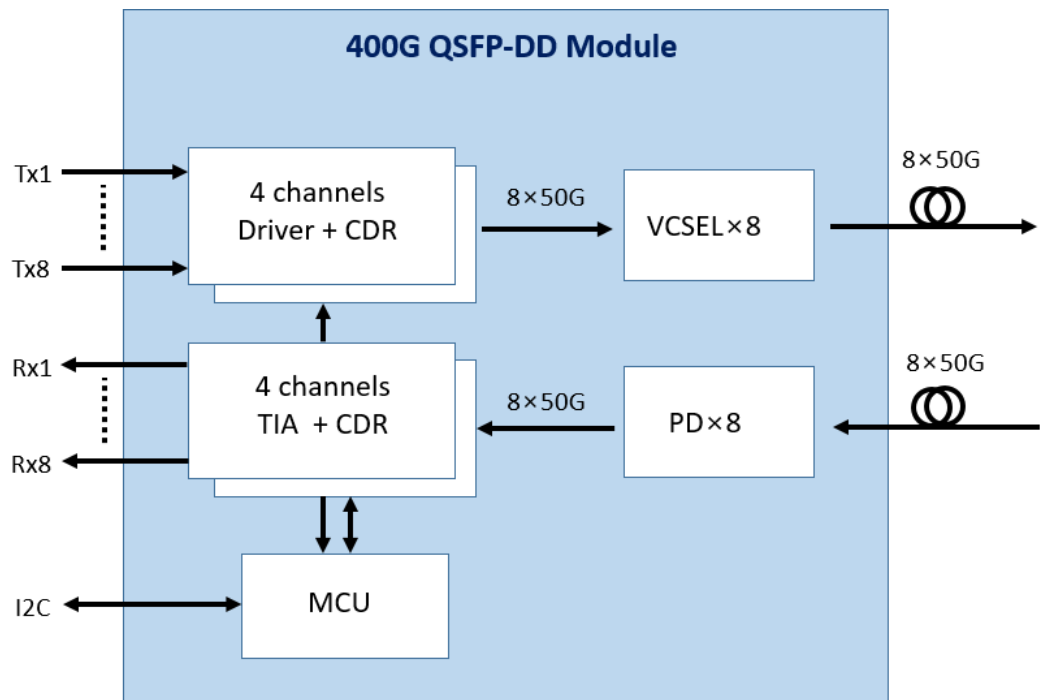
1. GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500 mA.
3. Not used

**Electrical Pin-out Details (QSFP56 100G End)**





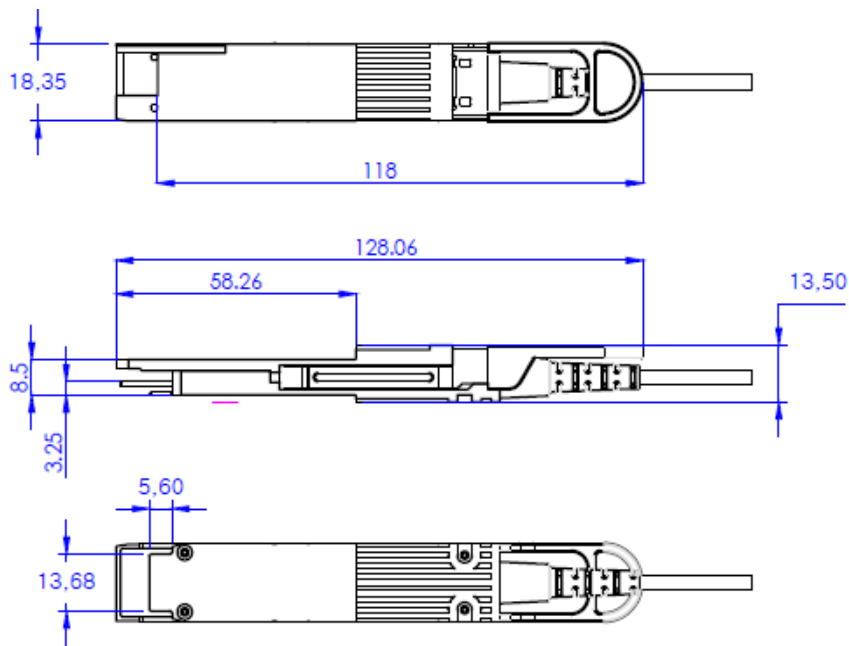
Block Diagram



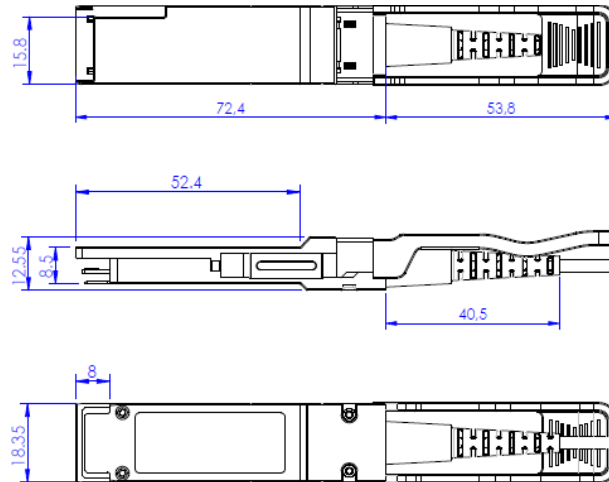
Active Optical Cable Specifications

| Parameter           | Value                            | Unit | Note            |
|---------------------|----------------------------------|------|-----------------|
| Cable Diameter      | LSZH: $\varnothing 3.0 \pm 0.15$ | mm   |                 |
| Minimum Bend Radius | 30                               | mm   | Without tension |
| Length Tolerance    | +300 / -0                        | mm   |                 |
| Cable Jacket        | LSZH, Aqua                       |      |                 |

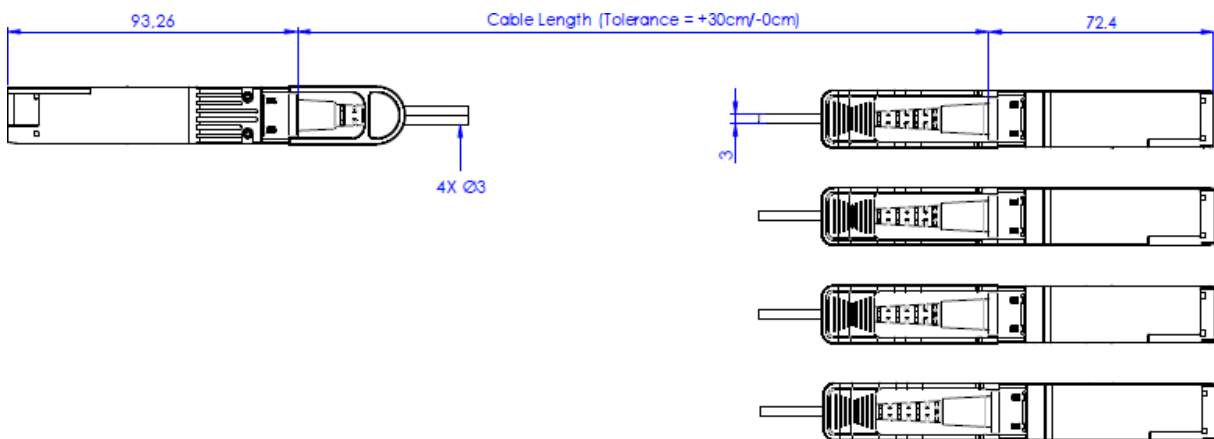
Mechanical Specifications



QSFP-DD 400G End



**QSFP56 100G End**



## **OptioConnect**

### **Innovation for the Future of High-Speed Networking**

#### **Who We Are**

OptioConnect is reshaping the landscape of communication and high-speed networking through intelligent technology. With a core focus on cutting edge technology, we deliver smarter fiber optic solutions for enterprise networks, data centers, and next-gen telecom infrastructures.

#### **What We Do**

At OptioConnect, we fuse advanced engineering with intelligent automation to drive the future of networking. Our AI-integrated solutions are designed to optimize performance and streamline operations with:

- Superior Performance
- Network and traffic optimization
- Intelligent energy management
- Seamless OEM compatibility
- Scalable cost-efficiency

#### **Smarter Networks by Design**

Innovation isn't just a goal—it's our process. We embed AI and machine learning across our R&D and product lines, enabling adaptive performance, automated tuning, and faster deployment cycles. The result? Networks that don't just work—they learn, evolve, and outperform.

#### **Our Team**

Our engineers, data scientists, and network architects bring decades of experience and a future-focused mindset. We provide hands-on support with intelligent insights that turn complex challenges into simple solutions.

#### **Our Mission**

To deliver AI-enhanced connectivity that reduces cost, increases speed, and maximizes efficiency—empowering our partners to operate at the forefront of a rapidly evolving digital world.

#### **Let's Connect**

Discover how OptioConnect's intelligent infrastructure solutions can power your network's next leap forward.

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