32GB DDR4-3200 UB-DIMM 1.2V

288pin PC4-25600 DDR4 Unbuffered DIMM Non-ECC

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32GB DDR4-3200 UB-DIMM

32G Bytes (4096M x 64 bits)
based on 16 pcs 2048M x 8 DDR4 SDRAM
288pin PC4-25600 DDR4 Unbuffered DIMM Non-ECC

Specifications

- RoHS Compliant (Lead Free) Memory module
- Density: 32GB
- Organization
  - — 4096M x 64 bits, 2 Rank
- Mounting 16 pieces of 16G bits DDR4 SDRAM sealed In FBGA
- Package: 288-pin, unbuffered dual in-line memory module (UDIMM)
  - — PCB height: 31.25mm
  - — PCB Gold Plating: 3u" min
- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- VDDSPD=1.7V to 3.6V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 internal banks
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Fast data transfer rates: PC4-25600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- CAS (READ) latency (CL): 14, 15, 16, 17, 18, 19, 21, 22
- On-Die Termination (ODT)
- Terminated control command and address bus
- Tcase of 0°C to 85°C (Components)
  - — 64ms, 8,192 cycle refresh at 0°C to 85°C
  - — 32ms at 85°C to 95°C
- Operating Temperature (Tcase)
  - — TOPR (Tcase) = 0°C ≤ TC ≤ +85°C
- Fly-by topology

Key Parameters

MT/s	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR4-3200	0.62	22	13.75	13.75	32	45.75	22-22-22

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0-A17[1]	Register address input	SCL	I^{2}C serial bus clock for SPD/TS and register
BA0, BA1	Regsiter bank select input	SDA	I^{2}C serial data line for SPD/TS and register
BG0, BG1	Regsiter bank group select input	SA0-SA2	I^{2}C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12V	Optional Power Supply on socket but not used on RDIMM
CKE0, CEK1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

1. Address A17 is only valid for 16Gbx4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Input/Output Functional Descriptions - Page1

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked compnent. Chip ID is considered part of the command code.
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t,NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/ TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing wherther to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also detemines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.

Input/Output Functional Descriptions - Page2

Symbol	Type	Function
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provied the row address for ACTIVATE Commands and the column address for Read/Write commands th select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active whenRESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, 12, 10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW.

Input/Output Functional Descriptions - Page3

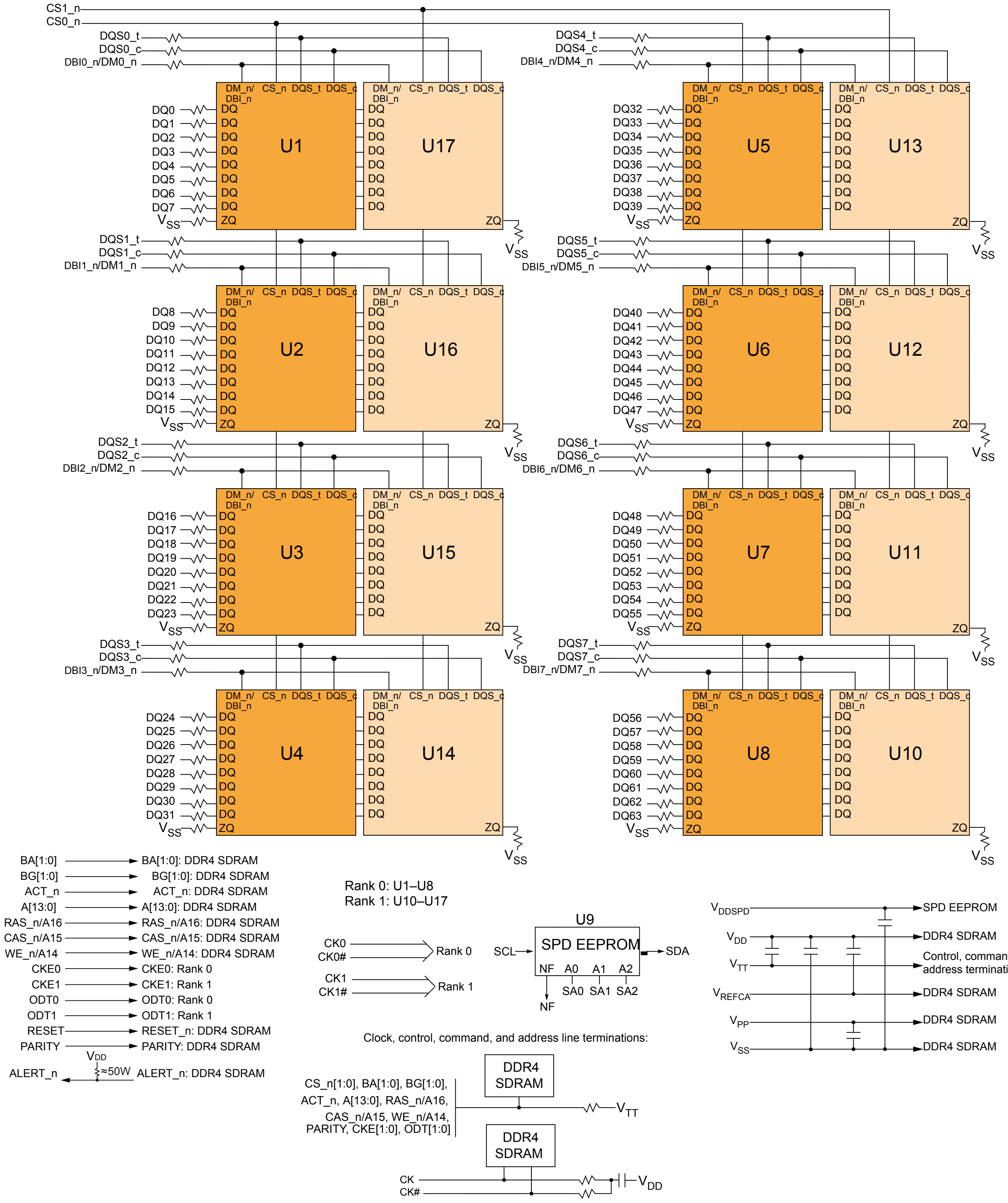
Symbol	Type	Function
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. IF there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete.
TEN	Input	Bourdary Scan Mode Enable: Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable boundary scan operation along with other pins. It is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.2 V +/- 0.06 V
V_{SS}	Supply	Ground
V_{pp}	Supply	DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Note: Input only pins (BG0-BG-1, BA0-BA1, A0-A17, ACT_n, RAS_n,/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

Pin Configurations

288-Pin DDR4 UDIMM Front								288-Pin DDR4 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	V_{SS}	73	V_{DD}	109	V_{SS}	145	NC	181	DQ29	217	V_{DD}	253	DQ41
2	V_{SS}	38	DQ24	74	CK0_t	110	DM5_n/DBI5_n, NC	146	V_{REFCA}	182	V_{SS}	218	CK1_t	254	V_{SS}
3	DQ4	39	V_{SS}	75	CK0_c	111	NC	147	V_{SS}	183	DQ25	219	CK1_c	255	DQS5_c
4	V_{SS}	40	DM3_n/DBI3_n, NC	76	V_{DD}	112	V_{SS}	148	DQ5	184	V_{SS}	220	V_{DD}	256	DQS5_t
5	DQ0	41	NC	77	V_{TT}	113	DQ46	149	V_{SS}	185	DQS3_c	221	V_{TT}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	EVENT_n, NF	114	V_{SS}	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DM0_n/DBI0_n, NC	43	DQ30	79	A0	115	DQ42	151	V_{SS}	187	V_{SS}	223	V_{DD}	259	V_{SS}
8	NC	44	V_{SS}	80	V_{DD}	116	V_{SS}	152	DQS0_c	188	DQ31	224	BA1	260	DQ43
9	V_{SS}	45	DQ26	81	BA0	117	DQ52	153	DQS0_t	189	V_{SS}	225	A10_AP	261	V_{SS}
10	DQ6	46	V_{SS}	82	RAS_n/A16	118	V_{SS}	154	V_{SS}	190	DQ27	226	V_{DD}	262	DQ53
11	V_{SS}	47	CB4/ NC	83	V_{DD}	119	DQ48	155	DQ7	191	V_{SS}	227	NC	263	V_{SS}
12	DQ2	48	V_{SS}	84	CS0_n	120	V_{SS}	156	V_{SS}	192	CB5, NC	228	WE_n/A14	264	DQ49
13	V_{SS}	49	CB0/ NC	85	V_{DD}	121	DM6_n/DBI6_n, NC	157	DQ3	193	V_{SS}	229	V_{DD}	265	V_{SS}
14	DQ12	50	V_{SS}	86	CAS_n/A15	122	NC	158	V_{SS}	194	CB1, NC	230	NC	266	DQS6_c
15	V_{SS}	51	DM8_n/DBI8_n, NC	87	ODT0	123	V_{SS}	159	DQ13	195	V_{SS}	231	V_{DD}	267	DQS6_t
16	DQ8	52	NC	88	V_{DD}	124	DQ54	160	V_{SS}	196	DQS8_c	232	A13	268	V_{SS}
17	V_{SS}	53	V_{SS}	89	CS1_n	125	V_{SS}	161	DQ9	197	DQS8_t	233	V_{DD}	269	DQ55
18	DMI_n/DBI1_n, NC	54	CB6/DBI8_n, NC	90	V_{DD}	126	DQ50	162	V_{SS}	198	V_{SS}	234	NC	270	V_{SS}
19	NC	55	V_{SS}	91	ODT1	127	V_{SS}	163	DQS1_c	199	CB7, NC	235	NC	271	DQ51
20	V_{SS}	56	CB2/ NC	92	V_{DD}	128	DQ60	164	DQS1_t	200	V_{SS}	236	V_{DD}	272	V_{SS}
21	DQ14	57	V_{SS}	93	NC	129	V_{SS}	165	V_{SS}	201	CB3, NC	237	NC	273	DQ61
22	V_{SS}	58	RESET_n	94	V_{SS}	130	DQ56	166	DQ15	202	V_{SS}	238	SA2	274	V_{SS}
23	DQ10	59	V_{DD}	95	DQ36	131	V_{SS}	167	V_{SS}	203	CKE1	239	V_{SS}	275	DQ57
24	V_{SS}	60	CKE0	96	V_{SS}	132	DM7_n/DBI7_n, NC	168	DQ11	204	V_{DD}	240	DQ37	276	V_{SS}
25	DQ20	61	V_{DD}	97	DQ32	133	NC	169	V_{SS}	205	NC	241	V_{SS}	277	DQS7_c
26	V_{SS}	62	ACT_n	98	V_{SS}	134	V_{SS}	170	DQ21	206	V_{DD}	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DM4_n/DBI4_n, NC	135	DQ62	171	V_{SS}	207	BG1	243	V_{SS}	279	V_{SS}
28	V_{SS}	64	V_{DD}	100	NC	136	V_{SS}	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DM2_n/DBI2_n, NC	65	A12/BC_n	101	V_{SS}	137	DQ58	173	V_{SS}	209	V_{DD}	245	DQS4_t	281	V_{SS}
30	NC	66	A9	102	DQ38	138	V_{SS}	174	DQS2_c	210	A11	246	V_{SS}	282	DQ59
31	V_{SS}	67	V_{DD}	103	V_{SS}	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V_{SS}
32	DQ22	68	A8	104	DQ34	140	SA1	176	V_{SS}	212	V_{DD}	248	V_{SS}	284	V_{DDSPD}
33	V_{SS}	69	A6	105	V_{SS}	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V_{DD}	106	DQ44	142	V_{PP}	178	V_{SS}	214	A4	250	V_{SS}	286	V_{PP}
35	V_{SS}	71	A3	107	V_{SS}	143	V_{PP}	179	DQ19	215	V_{DD}	251	DQ45	287	V_{PP}
36	DQ28	72	A1	108	DQ40	144	NC	180	V_{SS}	216	A2	252	V_{SS}	288	V_{PP}

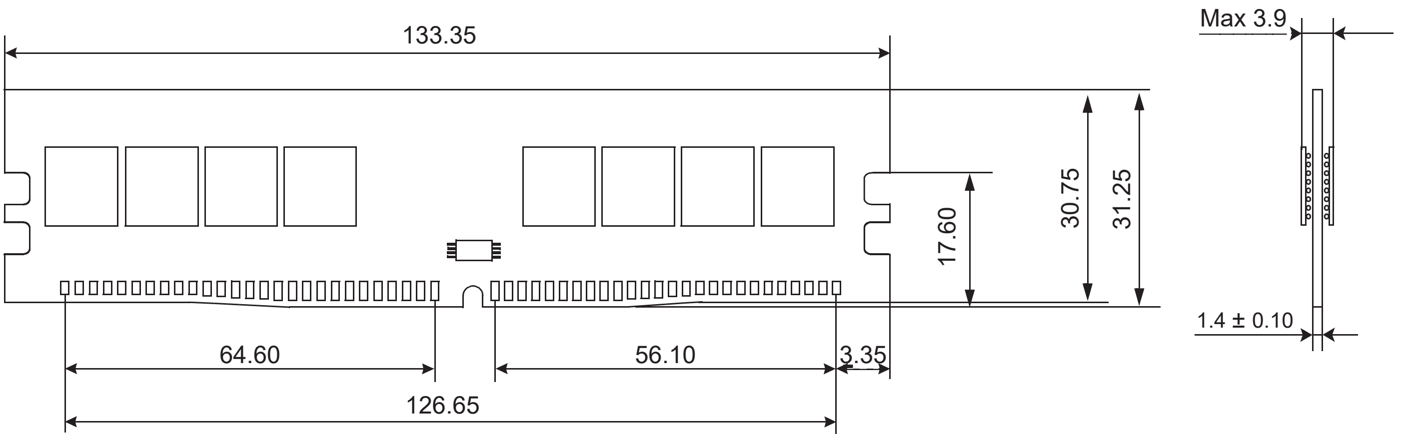
Functional Block Diagram



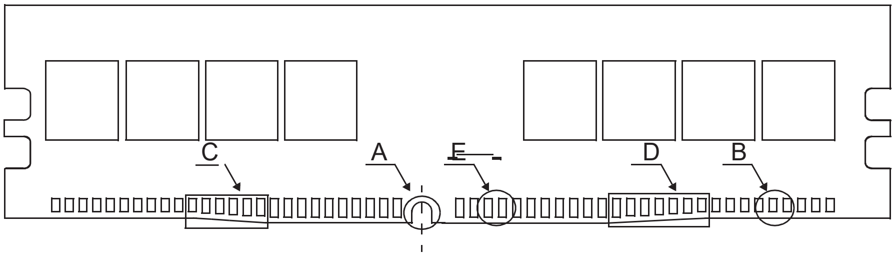
Note: 1. The ZQ ball on each DDR4 component is connected to an external 240 Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

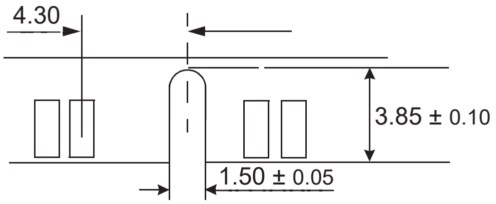
Physical Dimension

Front

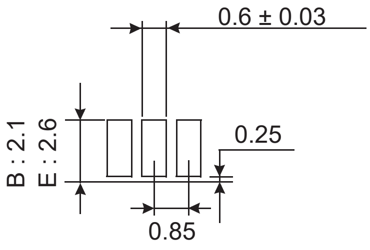


Back

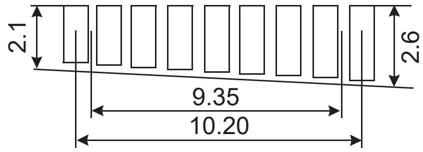




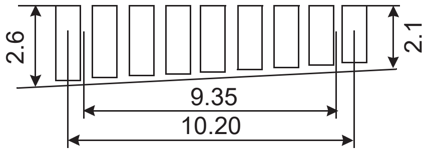
Detail A



Detail B,E



Detail C



Detail D

Note:

1. ±0.15 tolerance on all dimensions unless otherwise stated.

Units: millimeters